

Customer No.: 31561
Application No.: 10/711,838
Docket No.: 13869-US-PA

REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-15. Specifically, the Office Action rejected claims 1-2, 4-6 under 35 U.S.C. 103(a), as being unpatentable by Kropewnicki et al. (U.S. 6,440,864), as evidence by Wolf, Silicon Processing for the VLSI Era, Vol. 4, Lattice Press (2002). The Office Action also rejected claims 8-10, 12-14 under 35 U.S.C. 103(a) as being unpatentable over Kropewnicki in view of Mui (U.S. 2003/0228532). The Office Action rejected claims 3 and 11 under 35 U.S.C. 103(a) as being unpatentable over Kropewnicki in view of Wolf et al., Silicon Processing for the VLSI Era, Vol. 1, Lattice Press (1986). The Office Action rejected claims 7 and 15 under 35 U.S.C. 103(a) as being unpatentable over Kropewnicki in view of Wolf, Silicon Processing for the VLSI Era, Vol. 4, Lattice Press (2002).

No claim is amended, and claims 1-15 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

The Office Action rejected claims 1-2, 4-6 under 103(a) as being unpatentable over Kropewnicki et al. (U.S. 6,440,864), as evidence by Wolf, Silicon Processing for the VLSI Era, Vol. 4, Lattice Press (2002). Applicant respectfully traverses the rejections for at least the reasons set forth below.

To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined,

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must teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

The present invention is in general related an etching process as claim 1 recites:

Claim 1. An etching process, comprising:
providing a material layer having a bottom anti-reflection coating (BARC) and a patterned photoresist layer thereon;
etching the BARC using the patterned photoresist layer as a mask, wherein polymer as an etching by-product is formed on the patterned photoresist layer;
performing a cleaning step to remove the polymer from the patterned photoresist layer;
and
etching the material layer using the patterned photoresist layer as a mask, wherein the cleaning step is performed before the step of etching the material layer.

The Office Action stated Kropewnicki has disclosed performing a cleaning step to remove the polymer from the patterned photoresist layer at col. 3, lines 52-55; col. 6, lines 52-59. However, applicant respectfully disagrees. As a matter of fact, Kropewnicki teaches after the etching process, the etchant residue 60 along with remnant resist material 50 remaining on the substrate 30 must be removed to provide a clean substrate surface (see col. 3, lines 51-54). In other words, both of the etchant residue 60 and the resist material 50 are removed in the cleaning step. In addition, Kropewnicki also teaches the etchant residue 60 and the resist material 50 that remains on the substrate 30 after the etching process are removed in a cleaning chamber (see col. 3, lines 61-63). Moreover, Kropewnicki discloses process gas is introduced to remove the

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etchant byproducts 60 and remnant resist 50 on the substrate 30 at col. 6, lines 53-56. Therefore, in Kropewnicki reference, the cleaning step is used to remove both of the etchant residue 60 and the resist material 50. However, in claim 1 of the present application, the cleaning step is performed to remove the polymer from the patterned photoresist layer. That is, only the polymer is removed from the patterned photoresist layer in the cleaning step, and the patterned photoresist layer is not removed in the cleaning step. Because the patterned photoresist layer is not removed after the cleaning step, the patterned photoresist layer can be used as a mask for etching the underneath material layer subsequently.

The office action also stated Kropewnicki has disclosed that subsequent processing steps are performed at col. 3, lines 52-55, and Kropewnicki has also disclosed that forming integrated circuits involves etching silicon nitride,.....at col. 1, lines 5-15, and therefore from Fig. 1C, there is a suggestion that subsequent processing steps includes patterning polysilicon layer 40 with patterned resist layer 50. However, applicant respectfully disagrees. Please see Fig. 1C and col. 3, lines 51-54 of the Kropewnicki reference, the etchant residue 60 and the resist material 50 remaining on the substrate 30 are removed to provide a clean substrate surface. Therefore, there is not any resist material shown in Fig. 1C, and the layer 40 cannot be etched with the resist material 50 as a mask. If the layer 40 would be etched, the patterned dielectric layer 45 would be an etching mask. In addition please see Figs. 4A-4C of the citation, after the etchant residue 60 and the resist material 50 remaining on the substrate 30 are removed, the patterned dielectric layer 45 is used as an etching mask for patterning the layer 220 underneath so as to form a

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patterned layer 220 (shown in Fig. 4C). Therefore, the citation uses the dielectric layer as an etching mask that is much different from the present invention which using the photoresist layer as an etching mask. The feature of the present invention is performing a cleaning step to remove the polymer from the patterned photoresist layer, and then etching the material layer using the patterned photoresist layer as a mask. Because the polymer formed on the patterned photoresist layer is removed before etching the material layer, the pattern of the photoresist layer can be precisely transferred into the material layer. The objective of the present invention is to resolve the limitation of photolithograph process. The citation does not use photoresist layer as an etching mask, and thus the citation is different from the present invention in function, manner and result.

Moreover, Wolf also fails to teach or suggest the feature as above mentioned. Therefore, the two references combined do not teach each and every element in claim 1. For at least the foregoing reasons, Applicant respectfully submits a prima facie case of obviousness for claim 1 has not been established. Independent claim 1 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2, 4-6 patently define over the prior art as well.

The Office Action rejected claims 8-10, 12-14 under 103(a) as being unpatentable over Kropewnicki in view of Mui (U.S. 2003/0228532), rejected claims 3 and 11 under 35 U.S.C. 103(a) as being unpatentable over Kropewnicki in view of Wolf et al. (Silicon Processing for the

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VLSI Era, Vol. 1, Lattice Press (1986))(Wolf I) and rejected claims 1 and 2 as being unpatentable over Kropewnicki in view of Wolf. (Silicon Processing for the VLSI Era, Vol. 4, Lattice Press (2002))(Wolf IV). Applicant respectfully traverses the rejections for at least the reasons set forth below.

Applicant submits that, as disclosed above, Kropewnicki fails to teach or suggest each and every element of claim 1, from which claims 3 and 7-8 depend. Mui, Wolf I and Wolf IV also fail to teach the feature as above mentioned. Mui, Wolf I and Wolf IV cannot cure the deficiencies of Kropewnicki. Therefore, independent claim 1 is patentable over Kropewnicki, Mui, Wolf I and Wolf IV. For at the least the same reasons, its dependent claims 3 and 7-8 are also patentable as a matter of law.

The present invention also provides a patterning process as claim 9 recites:

Claim 9. A patterning process, comprising:
sequentially forming a bottom anti-reflection coating (BARC) and a photoresist layer on a material layer;
performing a lithography process to pattern the photoresist layer;
trimming the patterned photoresist layer;
etching the BARC using the patterned photoresist layer as a mask, wherein polymer as an etching by-product is formed on the patterned photoresist layer;
performing a cleaning step to remove the polymer from the patterned photoresist layer;
and
etching the material layer using the patterned photoresist layer as a mask, wherein the cleaning step is performed before the step of etching the material layer,
wherein the step of etching the BARC, the cleaning step and the step of etching the material layer are performed in-situ.

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As discussed above, Kropewnicki fails to teach or suggest that *performing a cleaning step to remove the polymer from the patterned photoresist layer and etching the material layer using the patterned photoresist layer as a mask, wherein the cleaning step is performed before the step of etching the material layer*. Mui also fails to teach this feature. Therefore, the references combined do not teach or suggest each and every element in claim 9, and thus independent claim 9 is patentable over Kropewnicki and Mui, and should be allowed. In addition, Mui, Wolf I and Wolf IV cannot cure the deficiencies of Kropewnicki. Therefore, independent claim 9 is patentable over Kropewnicki, Mui, Wolf I and Wolf IV.

In addition, in claim 9, the step of etching the BARC, the cleaning step and the step of etching the material layer are performed *in-situ*. However, Kropewnicki, Mui, Wolf I and Wolf IV also fails to teach the step of etching the BARC, the cleaning step and the step of etching the material layer are performed *in-situ*, and therefore, independent claim 9 is patentable over Kropewnicki, Mui, Wolf I and Wolf IV. For at the least the same reasons, its dependent claims 10-15 are also patentable as a matter of law.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,



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